Claims

1. A method in a memory device having a bank of N memory blocks, the method comprising the steps of:

generating an address for a first one of the N memory blocks as a current first possible refresh block and address for a current second one of the N memory blocks as a current second possible refresh block, for refreshing at least a portion of one of the possible refresh blocks;

checking for contention between the current first possible refresh block and an externally generated access to one of the N memory blocks; and

permitting the externally generated access to the one of the N memory blocks during a certain interval and refreshing the at least portion of the current first possible refresh block during the certain interval responsive to the memory block of the externally generated access not contending with the current first possible refresh block.

2. The method of claim 1 further comprising the step of permitting the externally generated access to the one of the N memory blocks during a certain interval, and refreshing the at least portion of the current second possible refresh block during the certain interval responsive to the following: i) the memory block of the externally generated access contending with the current first possible refresh block and, ii) the current first and second possible refresh blocks being different ones of the N memory blocks.

3. The method of claim 1 further comprising the steps of:

permitting the externally generated access to the one of the N memory blocks during a certain interval, and initiating an idle external access interval responsive to the following: i) the memory block of the externally generated access contending with the current first possible refresh

block, and ii) the current first and second possible refresh blocks being a same one possible refresh block; and

refreshing the one possible refresh block during the idle external access interval.

4. The method of claim 1 further comprising the steps of:

deferring the external access until a certain interval responsive to the following: i) the memory block of the externally generated access contending with the current first possible refresh block, and ii) the current first and second possible refresh blocks being a same one possible refresh block;

refreshing the one possible refresh block before the certain interval; and

permitting the externally generated access to the one of the N memory blocks during the certain interval.

5. The method of claim 1, wherein generating an address for the current first possible refresh block includes generating an address for a current portion of the current first possible refresh block, and wherein the method comprises the step of generating an address for a next portion of the current first possible refresh block responsive to the current portion not being a last portion of the current first possible refresh block.

6. The method of claim 5 further comprising the step of generating an address for a portion of a next first possible refresh block responsive to the current portion being a last portion of the current first possible refresh block.

7. The method of claim 2, wherein generating an address for the current second possible

refresh block includes generating an address for a current portion of the current second possible refresh block, and wherein the method comprises the step of generating an address for a next portion of the current second possible refresh block responsive to the current portion not being a last portion of the current second possible refresh block.

8. The method of claim 7 further comprising the step of generating an address for a portion of a next second possible refresh block responsive to the current portion being a last portion of the current second possible refresh block.

9. The method of claim 3, wherein generating an address for the current first possible refresh block includes generating an address for a current portion of the current first possible refresh block, and wherein the method comprises the step of generating an address for a next portion of the current first possible refresh block responsive to the current portion not being a last portion of the current first possible refresh block.

10. The method of claim 9, comprising the step of beginning a new refresh cycle for the bank of N memory blocks responsive to the current portion being a last portion of the current first possible refresh block.

11. A memory apparatus comprising:

a memory array segmented into N memory blocks;

first and second address generators, wherein the first address generator is operable to generate an address of a first one of the N memory blocks as a current first possible refresh block and the second address generator is operable to generate an address of a second one of the N memory blocks as a current second possible refresh block;

a multiplexer for receiving the current first possible refresh block and the current second possible refresh block from the respective address generators; and

external access compare logic operable to compare the block of an externally generated access to the current possible refresh block of the first address generator, wherein the apparatus is operable to permit the externally generated access to the one of the N memory blocks during a certain interval, and, the multiplexer is operable to select the at least portion of the current first possible refresh block for refreshing during the certain interval responsive to the external access compare logic indicating that the memory block of the externally generated access does not contend with the current first possible refresh block.

12. The apparatus of claim 11 further comprising:

refresh block compare logic operable for checking whether the first and second address generators are currently designating the same possible refresh block, wherein the apparatus is operable to permit the externally generated access to the one of the N memory blocks during the certain interval, and the multiplexer is operable to select the at least portion of the current second possible refresh block for refreshing during the certain interval responsive to i) the external access compare logic indicating that the memory block of the externally generated access contends with the current first possible refresh block and ii) refresh block compare logic indicating that the current

first and second possible refresh blocks are different ones of the N memory blocks.

13. The apparatus of claim 11 further comprising:

refresh block compare logic operable for checking whether the first and second address generators are currently designating the same possible refresh block; and

access control logic operable for initiating an idle external access interval responsive to i) the external access compare logic indicating that the memory block of the externally generated access contends with the current first possible refresh block and ii) refresh block compare logic indicating that the current first and second possible refresh blocks are a same one possible refresh block, so that the one possible refresh block may be refreshed during the idle external access interval.

14. The apparatus of claim 11 further comprising:

refresh block compare logic operable for checking whether the first and second address generators are currently designating the same possible refresh block; and

access control logic operable for deferring the external access to a certain interval responsive to i) the external access compare logic indicating that the memory block of the externally generated access contends with the current first possible refresh block and ii) refresh block compare logic indicating that the current first and second possible refresh blocks are a same one possible refresh block, so that the one possible refresh block may be refreshed before the certain interval and the external access may be performed during the certain interval.

15. The apparatus of claim 11, wherein the first address generator is operable to generate

an address for a current portion of the current first possible refresh block, and, responsive to the current portion not being a last portion of the current first possible refresh block, to generate an address for a next portion of the current first possible refresh block.

16. The apparatus of claim 15, wherein the first address generator is operable to generate an address for a portion of a next first possible refresh block responsive to the current portion being a last portion of the current first possible refresh block.

17. The apparatus of claim 12, wherein the second address generator is operable to generate an address for a current portion of the current second possible refresh block, and, responsive to the current portion not being a last portion of the current second possible refresh block, to generate an address for a next portion of the current second possible refresh block.

18. The apparatus of claim 17, wherein the second address generator is operable to generate an address for a portion of a next second possible refresh block responsive to the current portion being a last portion of the current second possible refresh block.

19. The apparatus of claim 13, wherein the first address generator is operable to generate an address for a current portion of the current first possible refresh block, and, responsive to the current portion not being a last portion of the current first possible refresh block, to generate an address for a next portion of the current first possible refresh block.

20. The apparatus of claim 19, wherein the first address generator is operable to initiate a new refresh cycle for the bank of N memory blocks responsive to the current portion being a last

portion of the current first possible refresh block.

21. A memory apparatus comprising:

a memory array segmented into N memory blocks;

first and second address generators, wherein the first address generator is operable to generate an address of a first one of the N memory blocks as a current first possible refresh block and the second address generator is operable to generate an address of a second one of the N memory blocks as a current second possible refresh block;

a multiplexer for receiving the current first possible refresh block and the current second possible refresh block from the respective address generators;

external access compare logic operable to compare the block of an externally generated access to the current possible refresh block of the first address generator, wherein the apparatus is operable to permit the externally generated access to access the one of the N memory blocks during a certain interval, and, the multiplexer is operable to select the at least portion of the current first possible refresh block for refreshing during the certain interval responsive to the external access compare logic indicating that the memory block of the externally generated access does not contend with the current first possible refresh block;

refresh block compare logic operable for checking whether the first and second address generators are currently designating the same possible refresh block, wherein the apparatus is operable to permit the externally generated access to access the one of the N memory blocks during the certain interval, and the multiplexer is operable to select the at least portion of the current second possible refresh block for refreshing during the certain interval responsive to i) the external access compare logic indicating that the memory block of the externally generated access contends with the current first possible refresh block and ii) refresh block compare logic indicating that the current

first and second possible refresh blocks are different ones of the N memory blocks; and

access control logic operable for initiating an idle interval responsive to i) the external access compare logic indicating that the memory block of the externally generated access contends with the current first possible refresh block and ii) refresh block compare logic indicating that the current first and second possible refresh blocks are a same one possible refresh block.

22. A method in a memory device having a bank of N memory blocks, the method comprising the steps of:

accessing any of N blocks of a memory array by external accesses;

refreshing a set of N-1 of the blocks, wherein responsive to contention arising between a particular external access to one of the N-1 blocks and refreshing of the block, an alternative one of the N-1 blocks is refreshed during the particular external access, so that contention between refreshing and external accessing is averted for the N -1 of the blocks in a cycle of completely refreshing all N blocks; and

refreshing the Nth block, including copying the Nth block to a buffer and permitting the external accesses concurrently with refreshing of the Nth block if i) the external accesses are not to the Nth block, or ii) the external accesses hit in the buffer.

23. The method of claim 22 comprising the step of :

refreshing a new N-1 set of the blocks while copying the buffer back to the Nth block of the previous set responsive to finishing the refreshing of the Nth block and there having been a hit in the buffer during the refreshing of the Nth block, wherein external accesses continue to be permitted concurrently with refreshing if i) the external accesses are not to the Nth block, or ii) the external accesses hit in the buffer.

24. The method of claim 23 comprising the steps of :

ceasing the copying of the buffer back to the Nth block and instead copying the Nth block to the buffer again responsive to i) finishing the refreshing of the new N-1 set of the blocks before finishing the copying of the buffer back to the Nth block of the previous set, and ii) the Nth block of the new set of the blocks being the same one of the blocks as the Nth block of the previous set.

25. The method of claim 23 wherein responsive to i) finishing the refreshing of the new N-1 set of the blocks before finishing the copying of the buffer back to the Nth block of the previous set, and ii) the Nth block of the new set of the blocks being a different one of the blocks than the Nth block of the previous set, the external accesses are permitted concurrently with refreshing only if the external accesses are not to the Nth block of the new set.

26. A memory apparatus comprising:

a memory array segmented into N memory blocks, wherein the memory array is accessed by external accesses during external access cycles;

a bi-directional refresh address generator for generating first and second addresses of the memory array for refreshing, wherein responsive to contention arising between an external access and refreshing at the first one of the refresh addresses, an alternative one of the N-1 blocks is refreshed using the second one of the refresh addresses, so that contention between refreshing and external accessing is averted for N -1 of the blocks in a cycle (a "memory bank refresh cycle") of completely refreshing all N blocks;

a data buffer; and

control logic, wherein responsive to the Nth block being reached in the memory bank refresh

cycle copying of the Nth block to the data buffer is initiated by the control logic, and if an external access hits in the data buffer the external access uses the data buffer instead of the Nth block, so that refreshing of the Nth block may proceed concurrently with external accesses during external access cycles when the external accesses and refreshes are not to the same block, and even during external access cycles when they are to the same block provided that the external accesses hit in the data buffer.

27. The memory apparatus of claim 26, wherein the control logic initiates refreshing a new N-1 set of the blocks and copying the buffer back to the Nth block of the previous set responsive to finishing the refreshing of the Nth block and there having been a hit in the buffer during the refreshing of the Nth block, and wherein external accesses continue to be permitted concurrently with refreshing if i) the external accesses are not to the Nth block, or ii) the external accesses hit in the buffer.

28. The memory apparatus of claim 27, wherein the control logic terminates the copying of the buffer back to the Nth block and initiates copying of the Nth block to the buffer again responsive to i) finishing the refreshing of the new N-1 set of the blocks before finishing the copying of the buffer back to the Nth block of the previous set, and ii) the Nth block of the new set of the blocks being the same one of the blocks as the Nth block of the previous set.

29. The memory apparatus of claim 27, wherein responsive to i) finishing the refreshing of the new N-1 set of the blocks before finishing the copying of the buffer back to the Nth block of the previous set, and ii) the Nth block of the new set of the blocks being a different one of the blocks than the Nth block of the previous set, the control logic permits external accesses concurrently with

refreshing only if the external accesses are not to the Nth block of the new set.